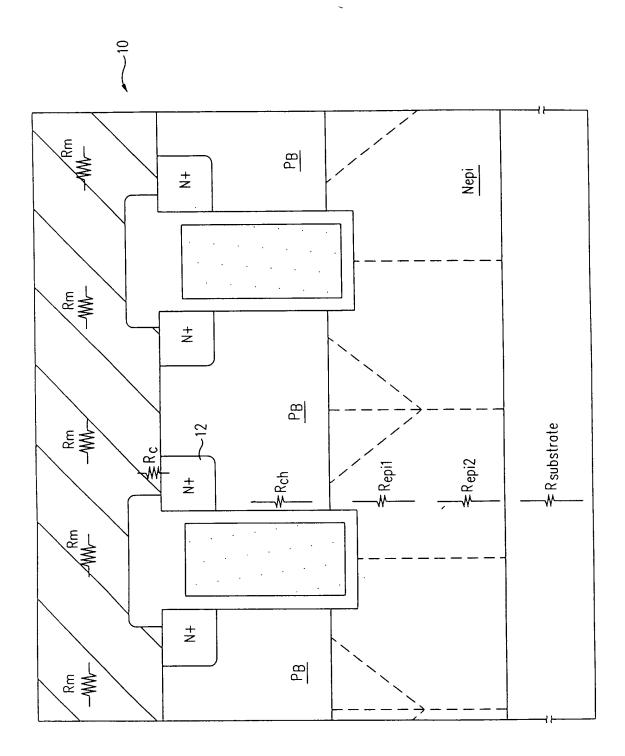
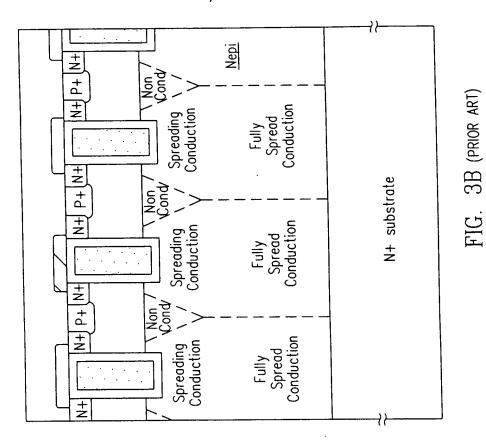


(PRIOR ART) FIG. 1



(PRIOR ART) FIG. 2

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Spreading Conduction Spreading Conduction

Fully Spread Conduction

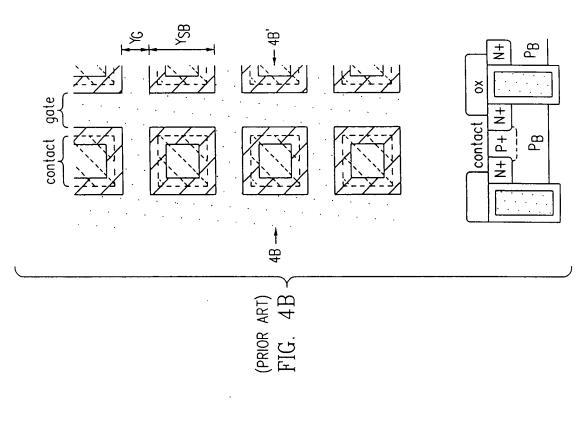
Non Spreading Conduction

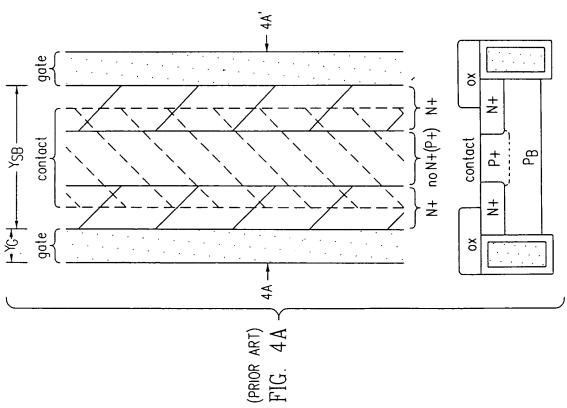
Nepi

Fully Spread Conduction

FIG. 3A (PRIOR ART)

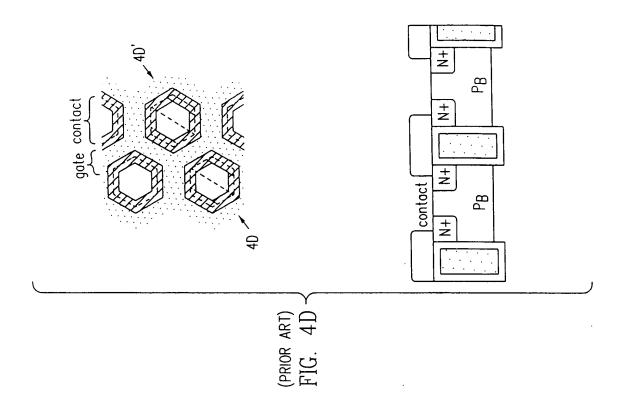
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 4 of 58

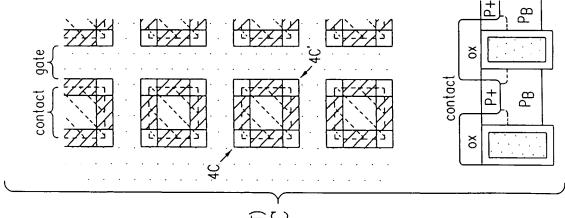




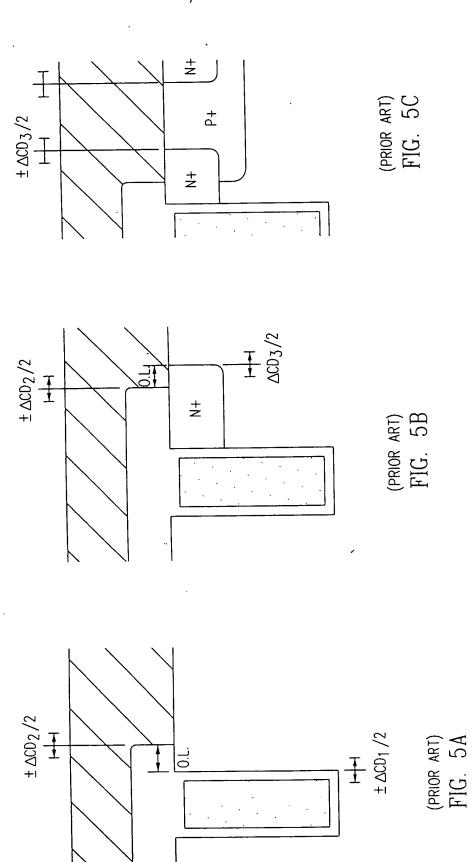
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 5 of 58

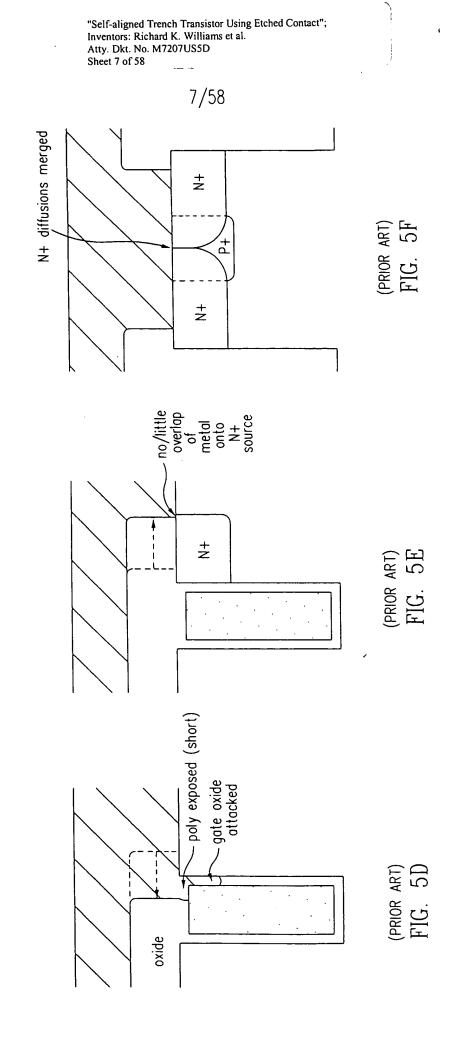
5/58



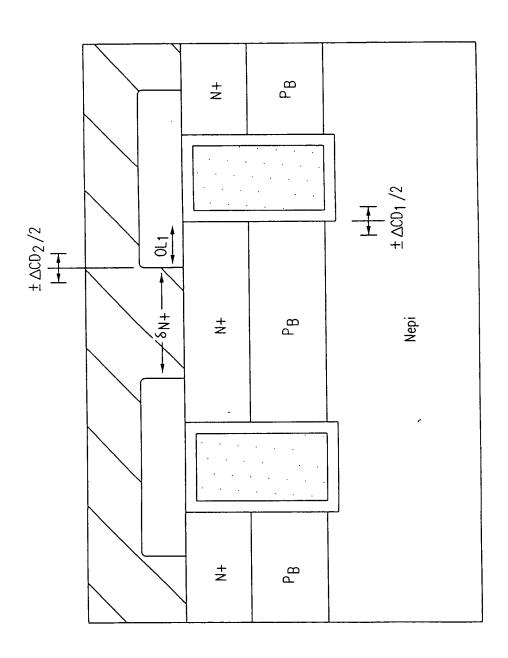


(PRIOR ART) FIG. 4C <





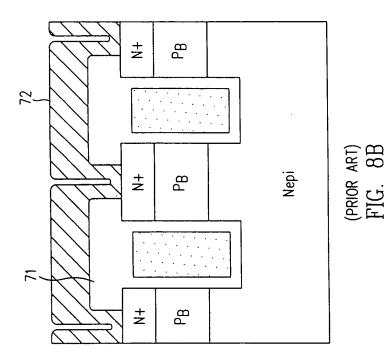
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 8 of 58

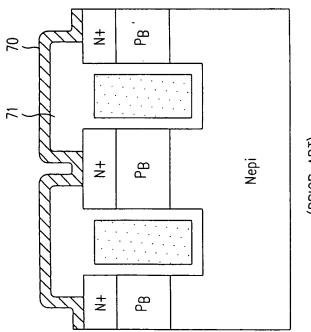


(PRIOR ART) FIG. 6

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 9 of 58 9/58 (PRIOR ART) FIG. 7B z direction (PRIOR ART) FIG. 7C 4 РВ z direction РВ ż N+ substrate (PRIOR ART) FIG. 7A ·Nepi РВ ŧ РВ ż

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 10 of 58

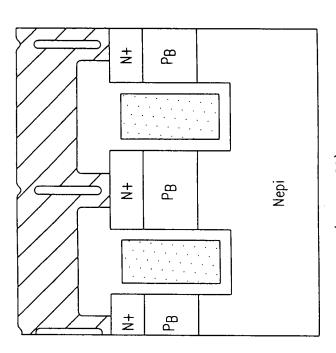




(PRIOR ART) FIG. 8A

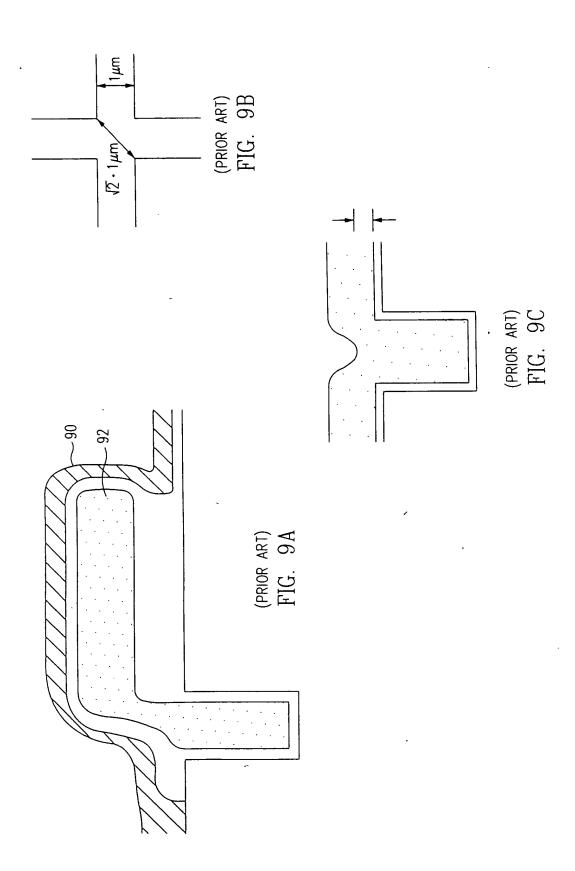
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 11 of 58

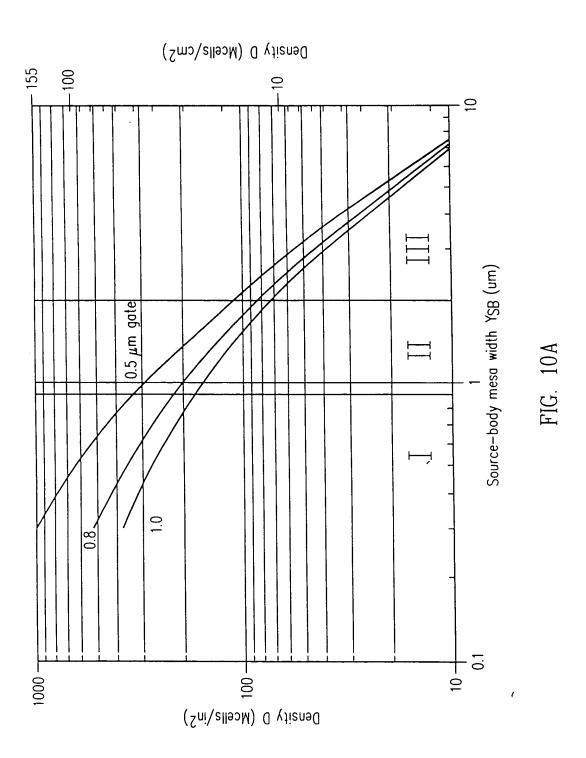
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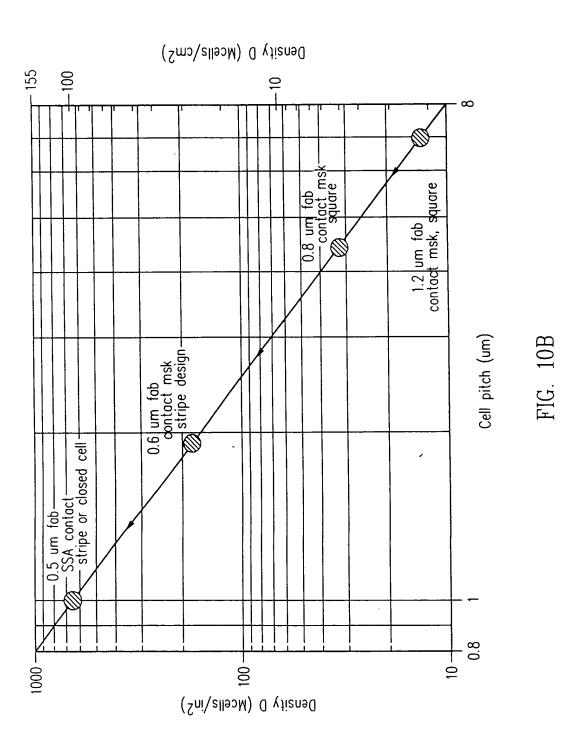


(PRIOR ART) FIG. 8C

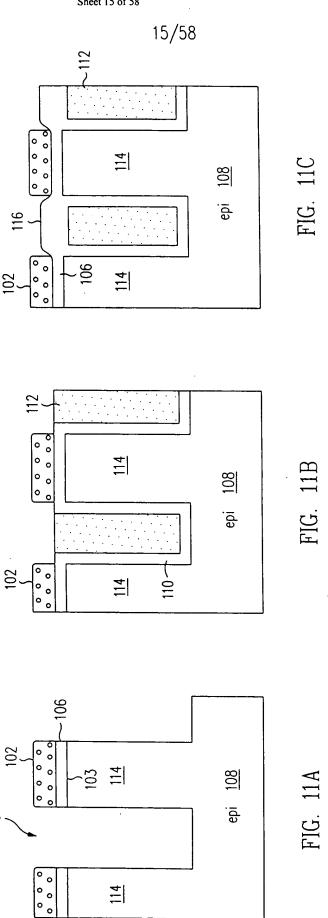
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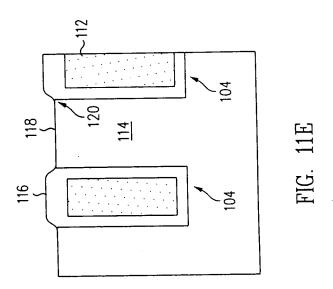


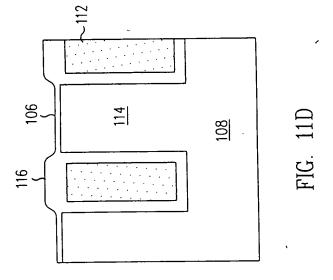
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD Sheet 15 of 58



"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 16 of 58

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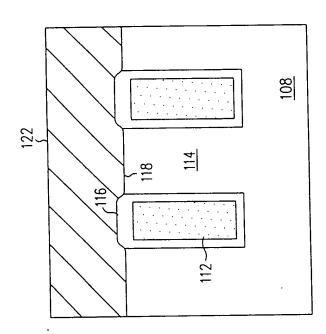
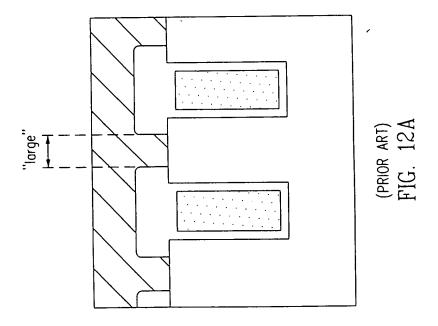
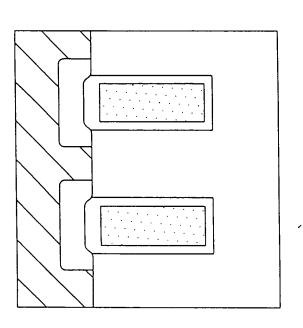
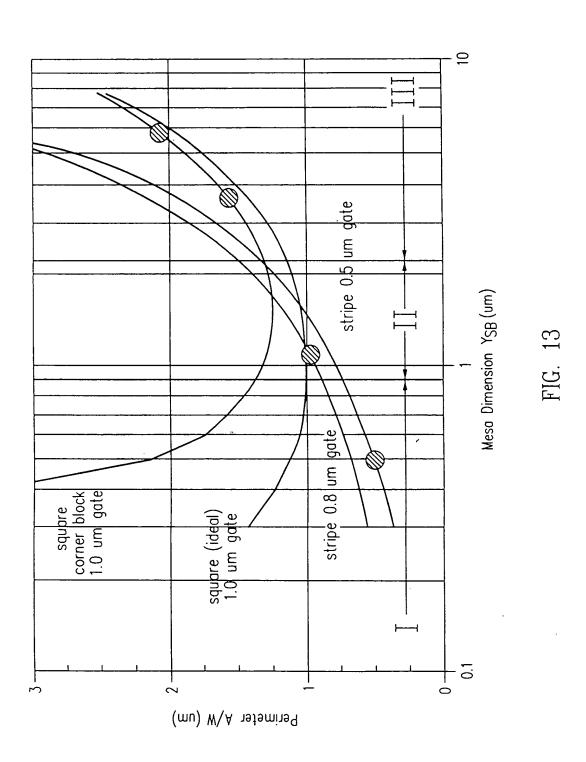


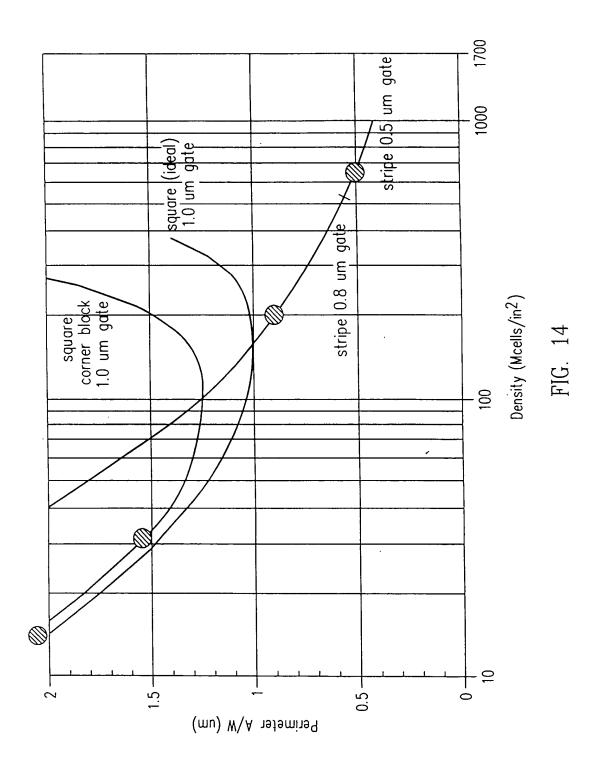
FIG. 12B



"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 18 of 58







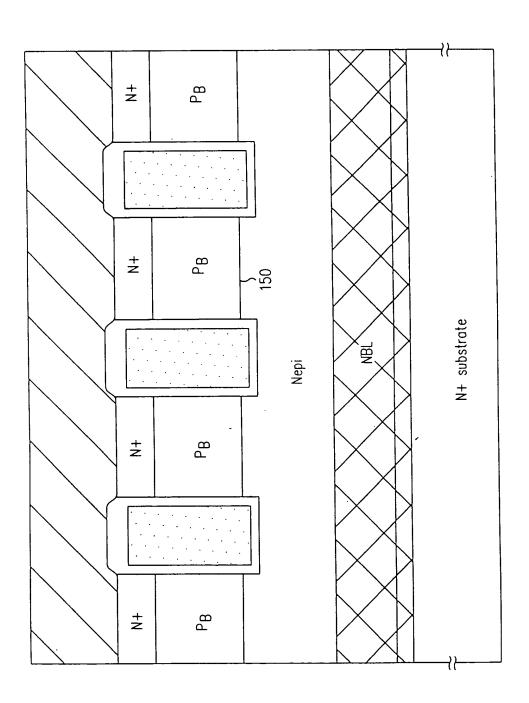


FIG. 15A

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 22 of 58

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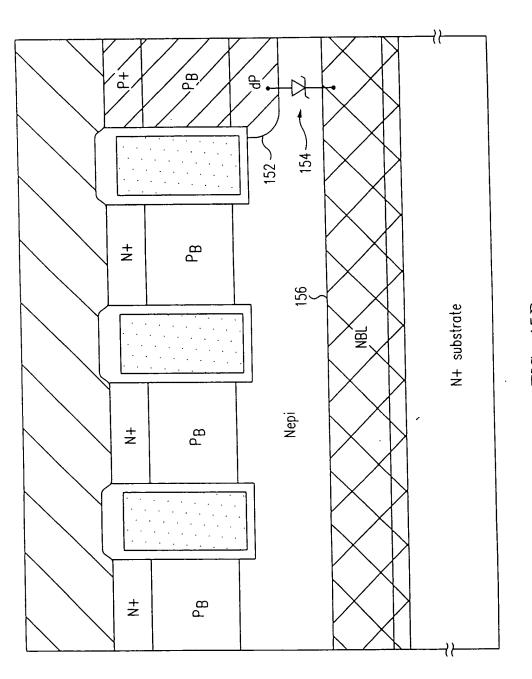
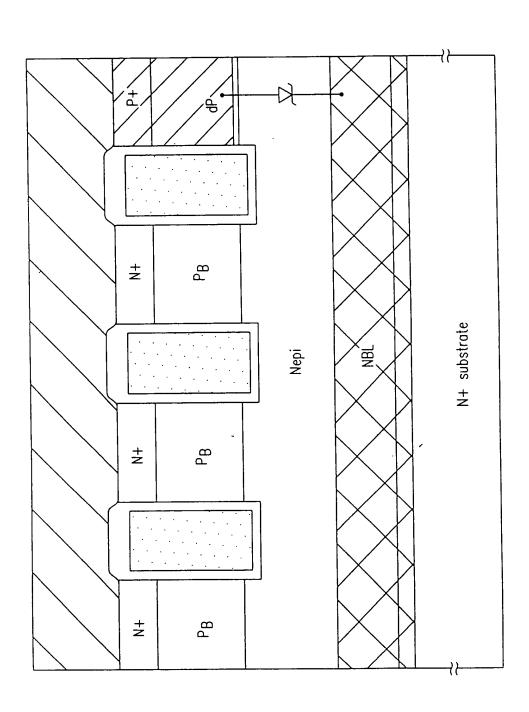


FIG. 15B

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 23 of 58



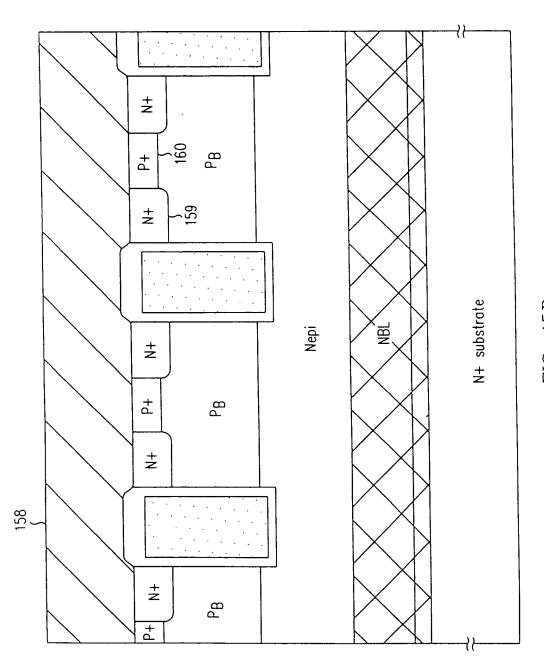
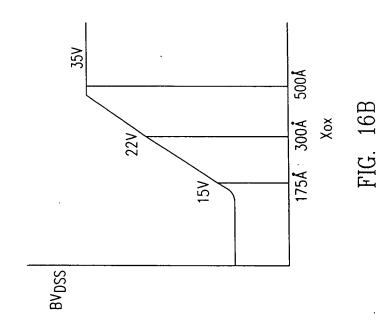
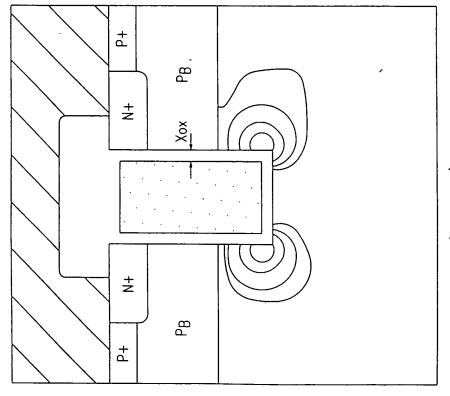


FIG. 15D

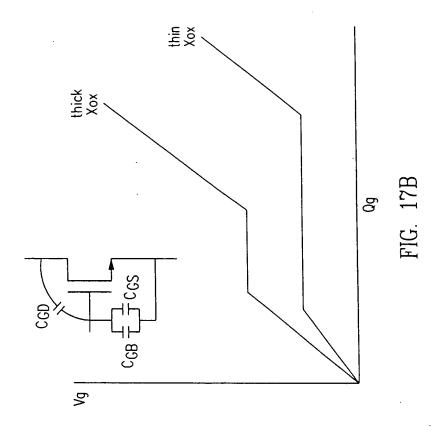
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 25 of 58





(PRIOR ART) FIG. 16A

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 26 of 58



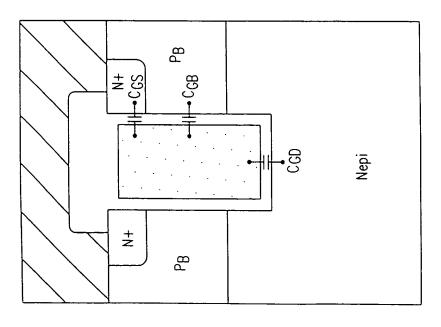


FIG. 17A

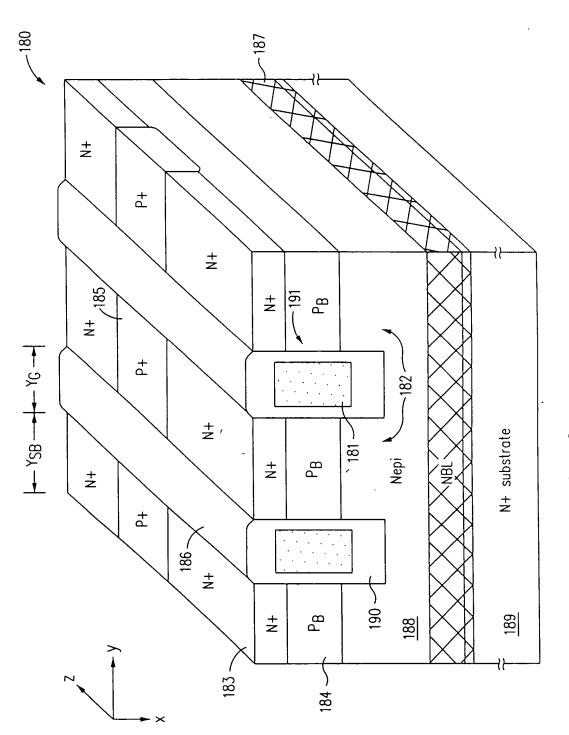
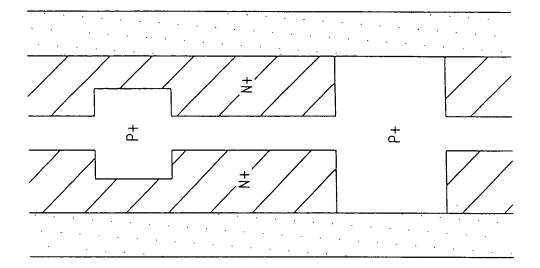
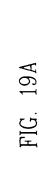


FIG. 18

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 28 of 58

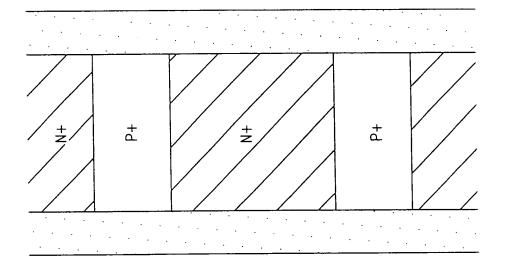
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þ‡ P+

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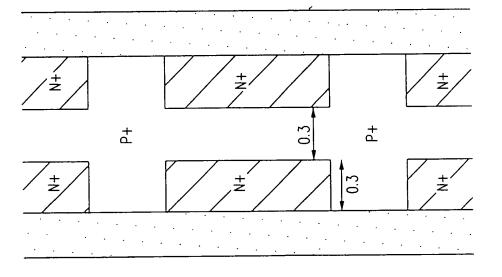
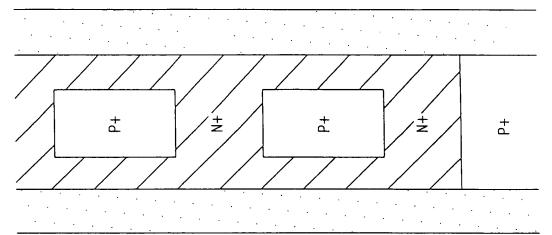


FIG 19D

FIG. 19C

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 30 of 58

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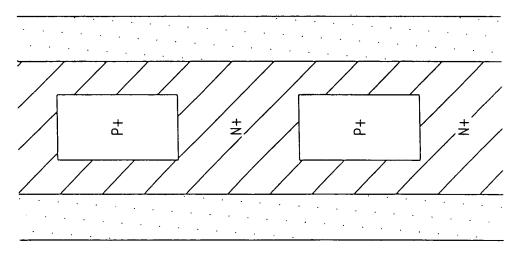
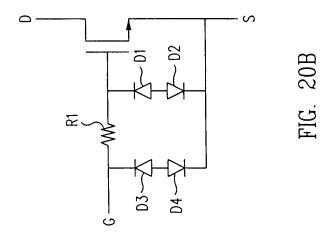
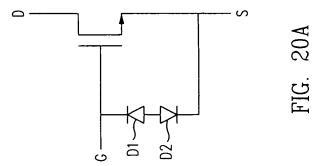
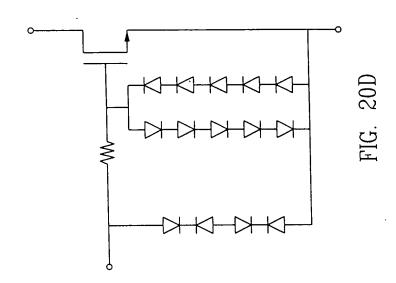


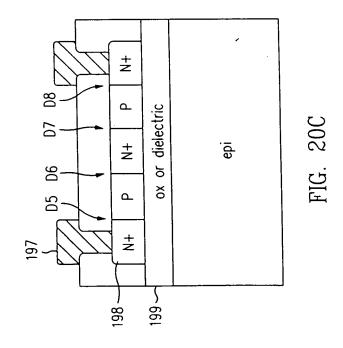
FIG 19F

리G. 19E

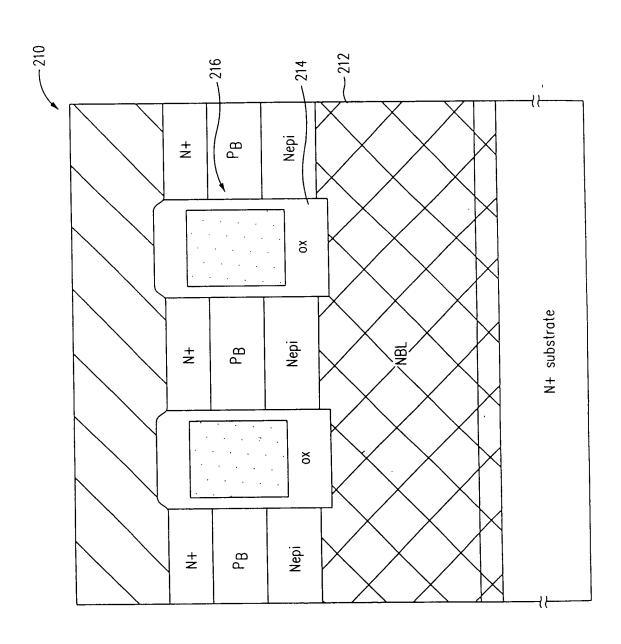








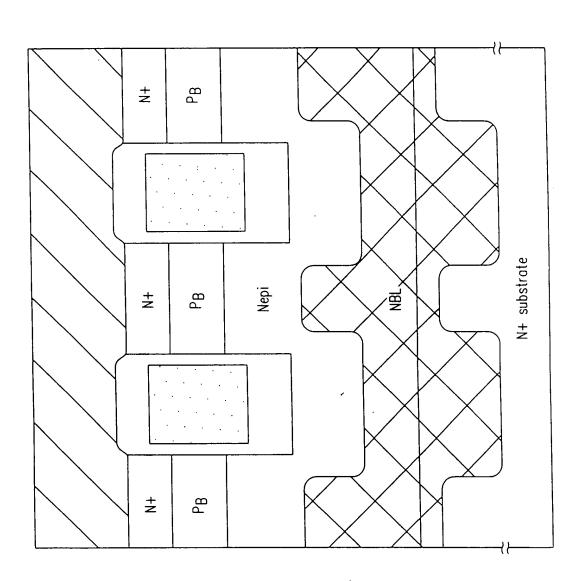
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 33 of 58



'IG. 21

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 34 of 58

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7G. 21H

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 35 of 58

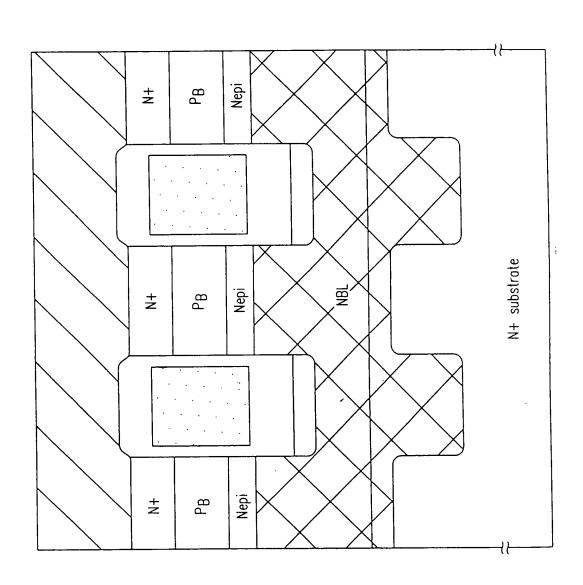


FIG. 22

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 37 of 58 37/58 267 294 300 299 295 291 292 293 -261N+ substrate FIG. 23 Nepi NB. 263 264 -278 275

265

278

-250

TERMINATION -290

269

268

source/body 302

303

281

288

gate

276

- ACTIVE ARRAY -260

→ CATE BUS → → POLY DIODE → 270

drain

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 38 of 58

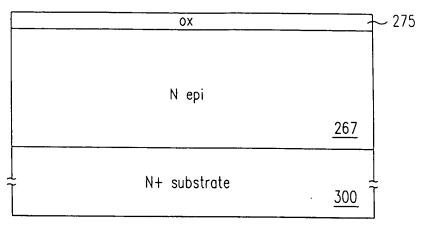


FIG. 24A

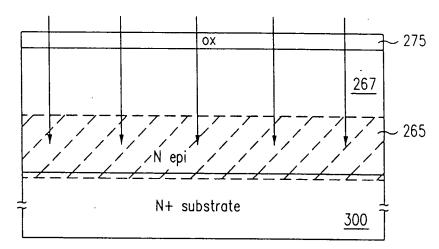


FIG. 24B

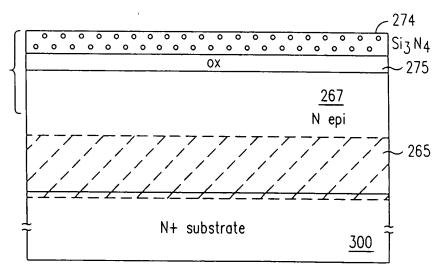


FIG. 24C

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 39 of 58

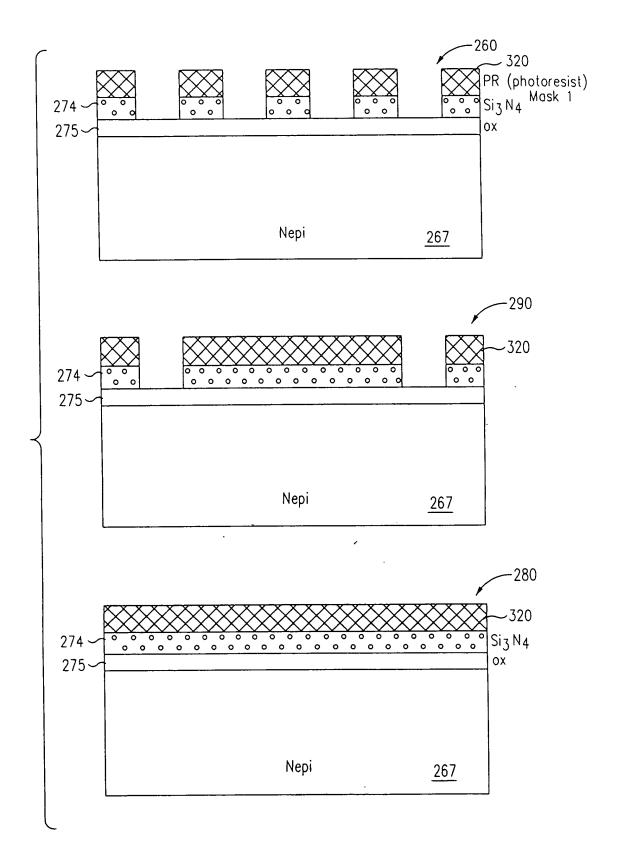


FIG. 24D

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 40 of 58

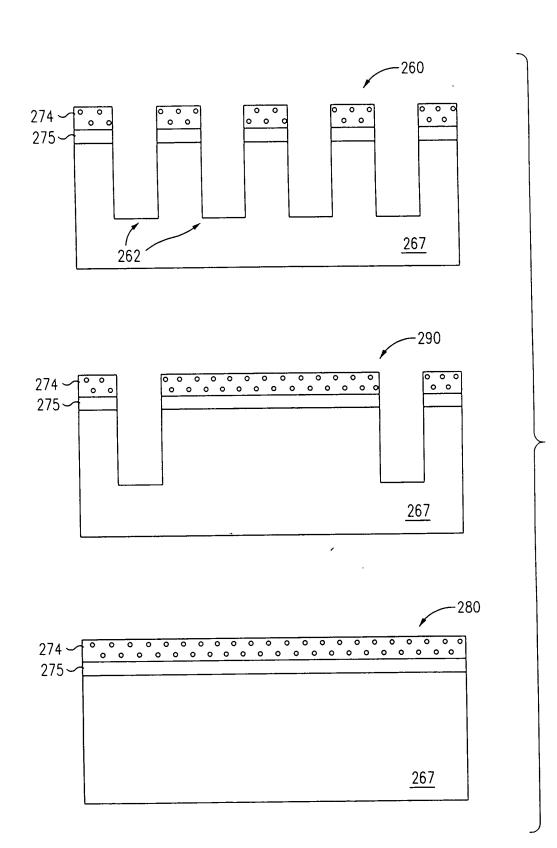


FIG. 24E

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 41 of 58

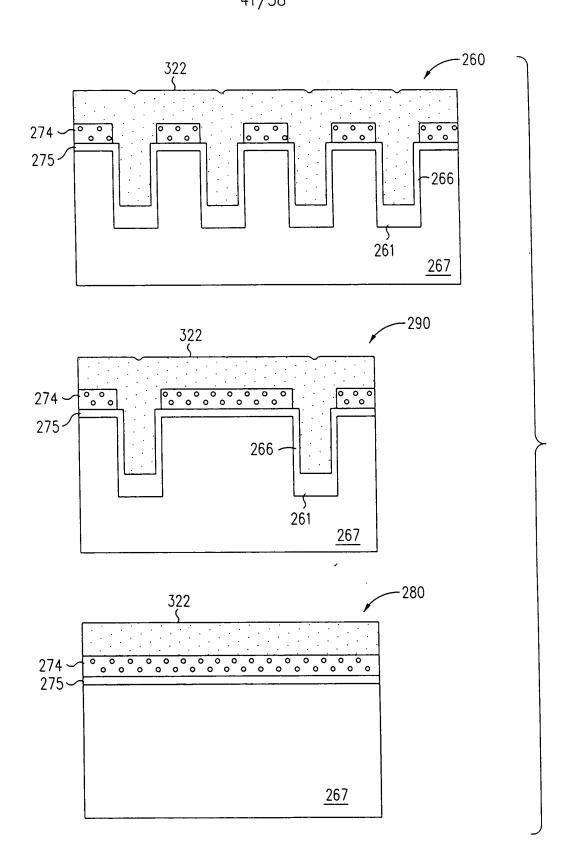


FIG. 24F

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 42 of 58

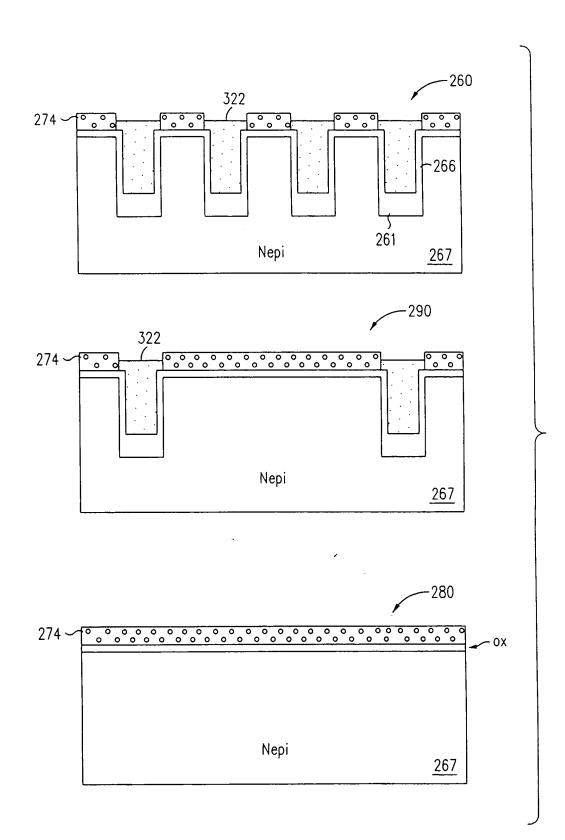


FIG. 24G

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD

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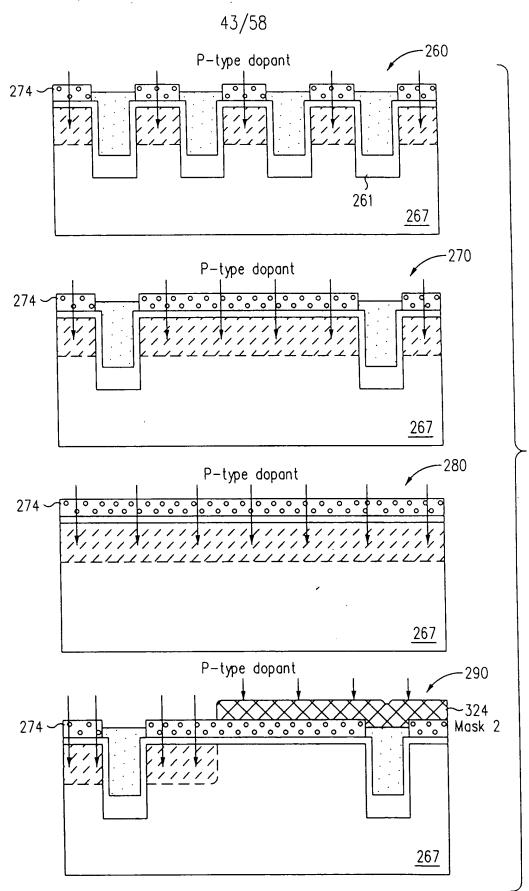


FIG. 24H

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 44 of 58

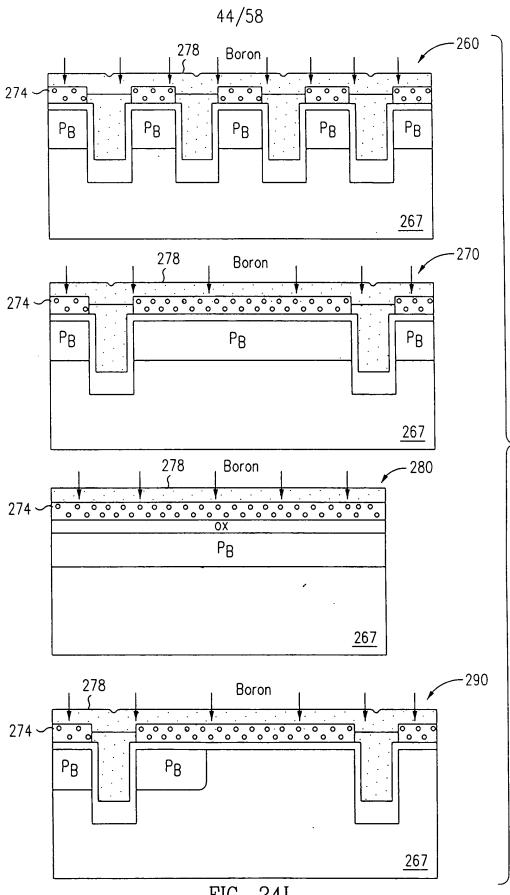


FIG. 24I

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 45 of 58

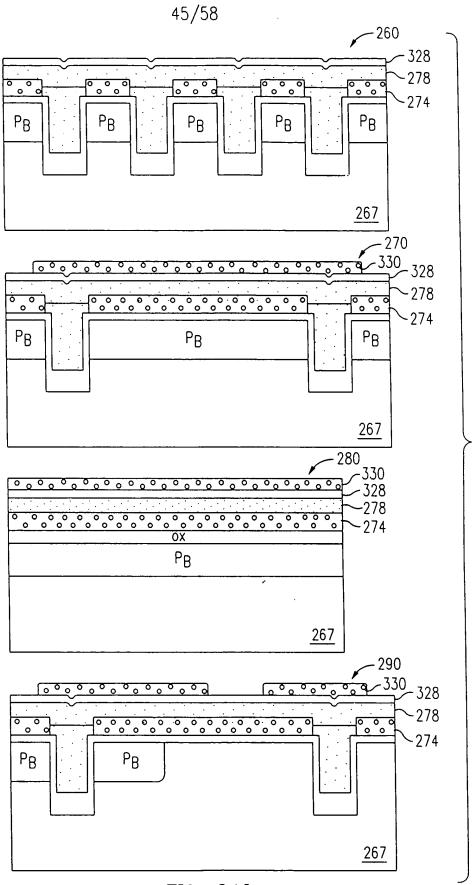


FIG. 24J

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 46 of 58

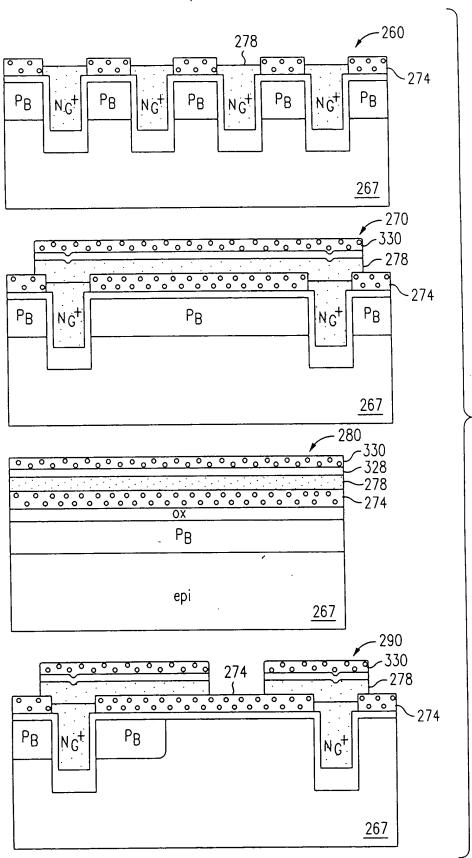


FIG. 24K

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 47 of 58

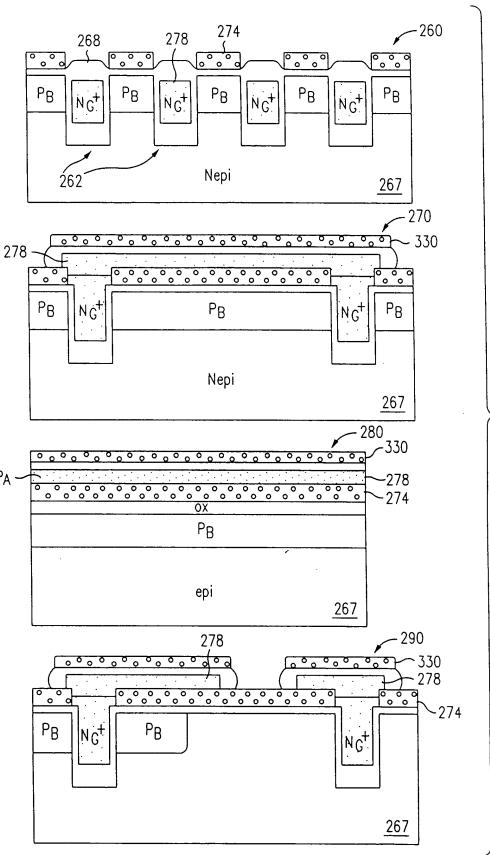


FIG. 24L

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 48 of 58

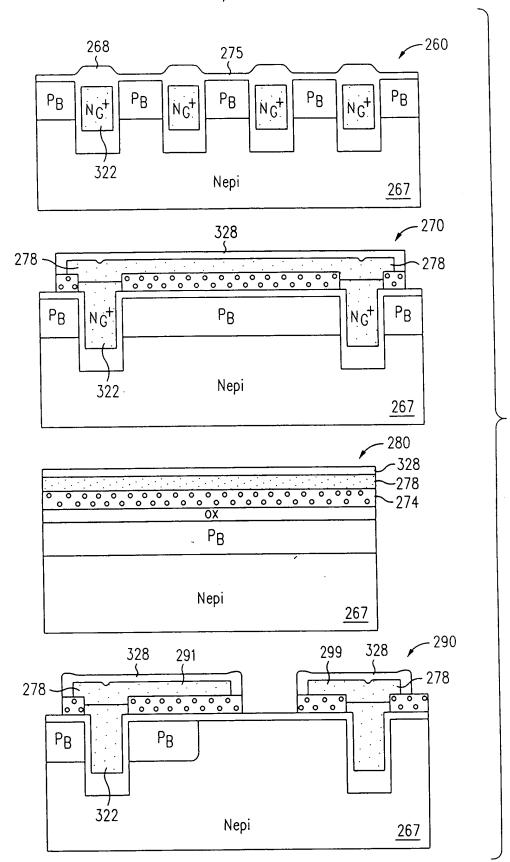


FIG. 24M

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD Sheet 49 of 58

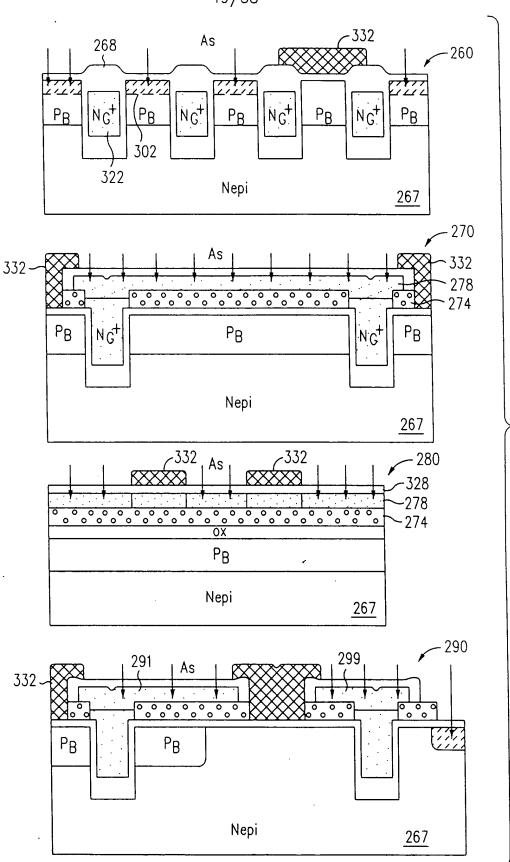


FIG. 24N

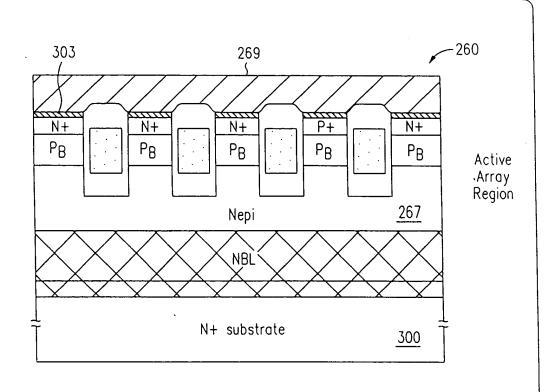
"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 50 of 58 50/58 BF<sub>2</sub> 260 N+  $NG^{+}$  $NG^{\dagger}$ NG+ Р<u>В</u> Active PB PB  $P_B$  $P_B$ Array Región Nepi <u> 267</u> 270 328 276 278 Gate РΒ NG+ PB Bus NG PB Region Nepi 267 280 BF<sub>2</sub> BF<sub>2</sub> 328 276 278 Poly Diode PB Region Nepi <u> 267</u> 290 276 278 **Termination** Region РΒ PB  $NG^{+}$ NG

FIG. 240

267

Nepi

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 51 of 58



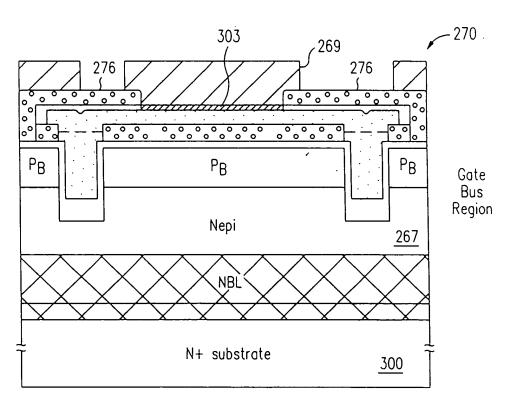
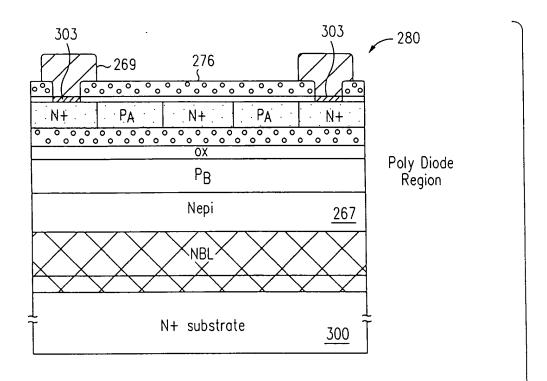


FIG. 24P

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD Sheet 52 of 58



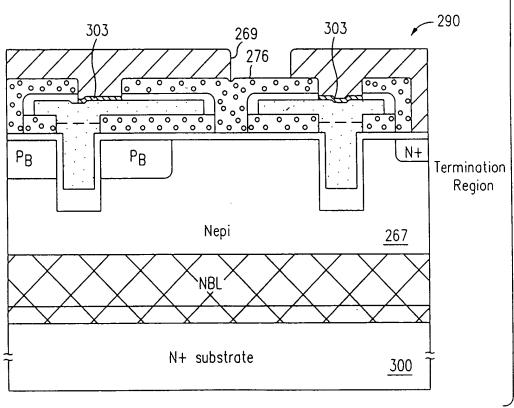
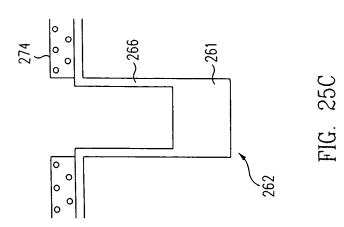
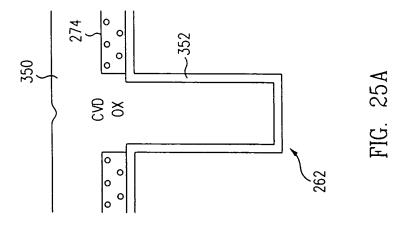


FIG. 24Q

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"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 54 of 58

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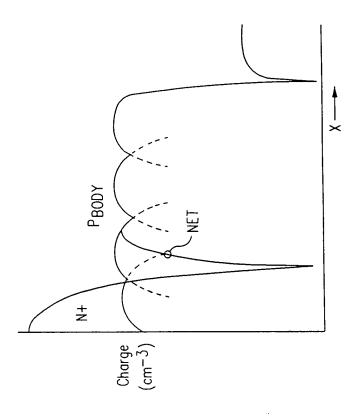
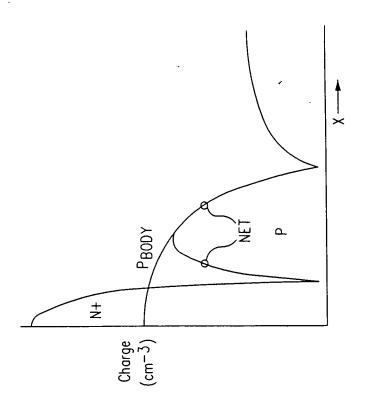
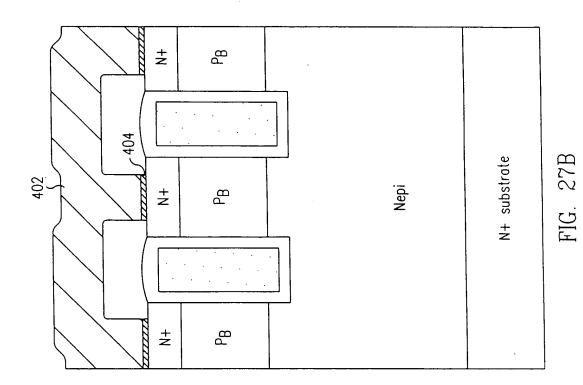


FIG. 26B

FIG. 26A



"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207US5D Sheet 55 of 58



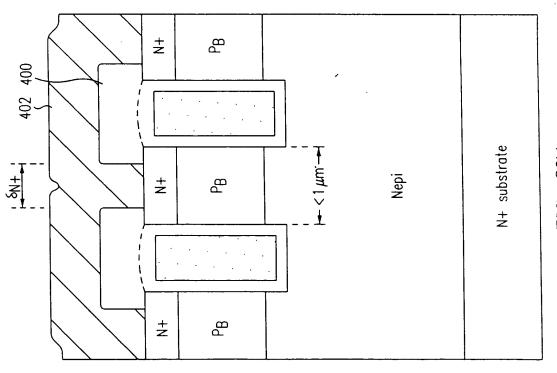
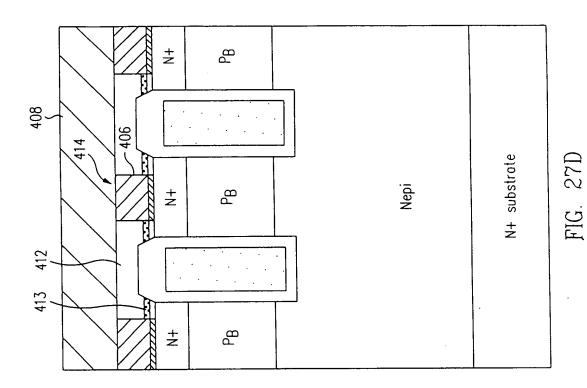


FIG. 27A



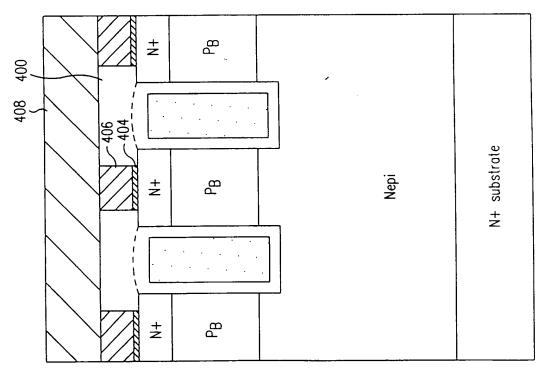


FIG. 27C

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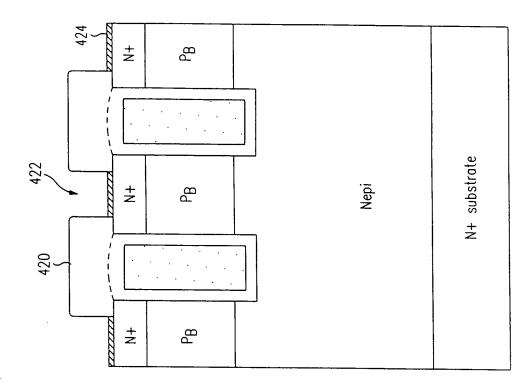


FIG. 28B

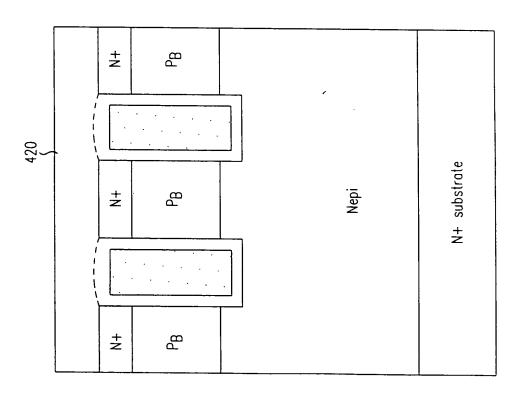
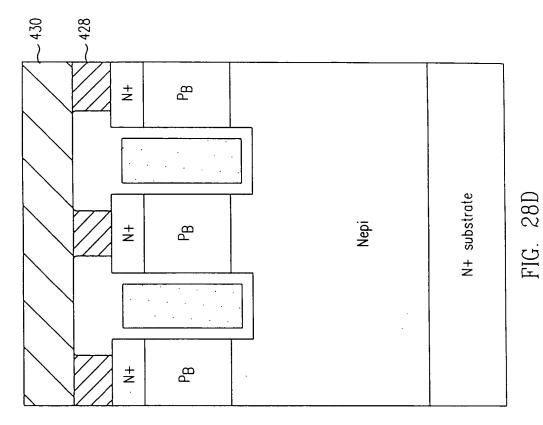


FIG. 28A

"Self-aligned Trench Transistor Using Etched Contact"; Inventors: Richard K. Williams et al. Atty. Dkt. No. M7207USSD Sheet 58 of 58



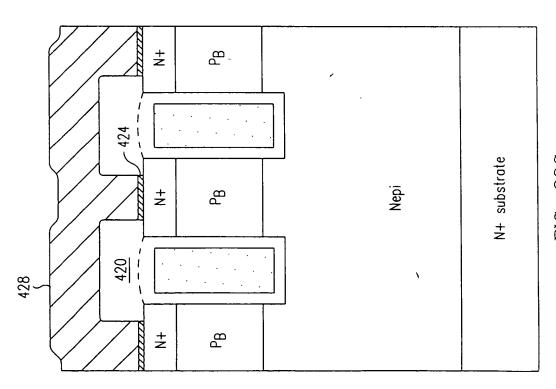


FIG. 28C